REMARKS

Claims 1-2, 9, 18 and 25 are amended. Claims 7, 16, 23, and 30 are canceled. Claims 1-6, 8-15, 17-22, and 24-29 are pending.

Prior Art Rejections under 35 U.S.C. Section 102

Claim 1 of the application recites a method that includes automatically upgrading internal software of a peripheral device installed in a network device using an upgrade package. The upgrade package includes a flash erase file for erasing the contents of memory in the peripheral device as well as software for updating the peripheral device. An example is discussed in connection with FIG. 4 of the specification. In that example, an upgrade package 60 is provided that contains both a flash erase file 64 and new software 62 that are used during a peripheral device upgrade. For example, as disclosed on page 4 of the specification, the flash erase file 64 is used to erase existing software in the peripheral device and sets the peripheral device to a mode wherein the new software 62 can be written to the peripheral device. Independent claims 9 and 18 also recite an upgrade package with a flash erase file.

Claims 1-6, 8-15, 17-22, and 24-29 stand rejected as anticipated by the Deegan et al. patent. The Deegan et al. patent discloses a method and apparatus for transferring firmware to a non-volatile memory of a programmable controller system. The method disclosed in Deegan et. al., for upgrading the peripheral devices, however, is different from what is claimed in the current invention. The Deegan et. al patent describes the transfer process to the peripheral device as follows:

> Step S6 establishes an outer loop for the performance of steps S7-S14, and step S7 establishes an inner loop for the performance of steps S8-S11. During the inner loop, blocks are transferred from the random access memory 26 by way of dual port RAM 37. When enough blocks have been transferred such that the random access memory 26 is full (J=N), then the portion of the firmware upgrade contained in the random access memory 26 is burned into the non-volatile memory 24 using conventional non-volatile

memory programming techniques. This process is repeated until the entire firmware upgrade has been burned into the non-volatile memory 24 (I=M).

(Col. 8, lines 41 – 55, emphasis added)

Deegan et. al. does not suggest or teach the use of a flash erase file to erase memory locations of a peripheral device. Furthermore, Deegan et. al does not suggest or teach the use of a flash erase file during an upgrade of a peripheral device.

In view of the foregoing remarks, applicant respectively requests withdrawal of the rejections of claims 1-6, 8-15, 17-22, and 24-29.

Prior art rejections under 35 U.S.C. Section 103

Claims 8, 17 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Deegan et. al., in view of U.S. Patent 6,601,212 to Guha et. al. The Guha et. al. patent also does not disclose or suggest the claim limitations missing from the Deegan et. al. patent. In particular, there is no suggestion that the upgrade process disclosed in the Guha patent utilizes a flash erase file to prepare the peripheral device for an upgrade. For at least this reason, applicant respectively requests withdrawal of the rejections of claims 8, 17 and 24.

Conclusion

In view of the foregoing remarks, applicant respectfully requests allowance of the claims.

Please apply any charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10830-079001.

Respectfully submitted,

Date: 2/9/04

Samuel Borodach
Reg. No. 38,388

Attorney for Intel Corporation
Fish & Richardson P.C.
4350 La Jolla Village Drive
Suite 500
San Diego, CA 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099